UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,552	02/27/2002	Hiroshi Nakamura	001701.00672	8483

22907 7590 06/14/2002

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	3

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/083,552	NAKAMURA, HIROSHI	
	Examiner	Art Unit	
	Quan Tra	2816	MC

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/656,831* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. Claims 1-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-12 of U.S. Patent No. 6373327. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claims 1-12 disclose all of elements of the applicant claims 1-9. With respect to patent claims 1-12, it discloses a voltage generating/transferring circuit having boost unit group, first transistor... Applicant claims 1-9 discloses a voltage generating/transferring circuit having boost unit group, first transistor ... Since the voltage generating/transferring circuit of the patent claims 1-12 performs all of the required functions of the voltage generating/transferring circuit of the applicant claims 1-9, it would have been obvious to a skilled artisan to use voltage generating/transferring circuit of the patent claims 1-12 to provide the necessary voltage generating/transferring circuit.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is indefinite because it is unclear as to where the "second voltage" is generated from of applied to.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3-6are rejected under 35 U.S.C. 102(b) as being anticipated by Bill et al. (USP 5059815).

As to claim 1, Bill et al. discloses in figure 1a a circuit comprising: a boost unit group including a plurality of boost units (110, 140) series-connected between input and output nodes (Vout); a first transistor (100) connected between the input node and a node for receiving a first voltage (Vpp); and a capacitor (CL) connected to the output node, wherein each boost unit has input and output portions, and includes a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a capacitor (120, 130) connected to the input portion, and a gate of said first transistor is connected to the output node.

Insofar as understood to claim 3, figure 2 shows a third transistor (250) which has a gate connected to the output node, and transfers a third voltage, wherein a second voltage (VppI) is equal to, or larger than a sum of the third voltage and a threshold voltage of said third transistor.

As to claim 4, figure 1A shows a first oscillation signal Φ is input to an even-numbered boost unit from the input node, a second oscillation signal ϕ is input to an odd-numbered boost unit from the input node, and the first and second oscillation signals have opposite phases or different timings (see figure 1B).

As to claim 5, it is inherent for gate and source voltage levels of said first transistor gradually rise while changing in opposite phases.

As to claim 6, figure 1a shows a circuit (160) for fixing the gate of said first transistor to low level in an OFF state.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bill et al. (USP 5059815).

As to claim 2 Bill et al.'s figure 1a shows all limitations of the claim except for the boost unit group includes not less than three boost units. However, the selection for the boost unit to have not less than three boost units is seen as a matter of design choice depending on the design output level voltage (the more stage the higher output level), column 3, lines 15-25 also teaches number of boosting unit is a matter of design choice.

As to claims 7-9, figures 1a shows all limitations of the claims except for a threshold voltage of the second transistor in at least one of the boost units is lower than a threshold voltage of the first transistor; or a transistor having a threshold voltage lower than the threshold voltage of the first transistor is arranged in a boost unit closest to the output node; a threshold voltage of a transistor in a boost unit on the output node side is lower than a threshold voltage of a transistor in a boost unit on the input node side. However, it is well known in the art that threshold of the

diode connected transistors e.g. 350, 360... determined the level of the voltage output. Therefore, it would have been obvious to one having skill in the art to select the threshold of all diode connected transistors in the boost unit to be less than the threshold of the first transistor for the purpose of reducing the output voltage level.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
June 4, 2002

Terry D. Cunningham
Primary Examiner